Remarks

Applicant respectfully requests that this Amendment After Final Action be admitted under 37 C.F.R. § 1.116.

Applicant submits that this Amendment presents claims in better form for consideration on appeal. Furthermore, applicant believes that consideration of this Amendment could lead to favorable action that would remove one or more issues for appeal.

Claims 1, 8, 9, 20, 21 and 24 have been amended. No claims have been canceled. Therefore, claims 1-24 are now presented for examination.

In the Final Office Action, the Examiner has objected to the title of the invention. Applicants submit that the title has been amended as suggested by the Examiner.

Claims 1-3, 8-24 stand rejected under 35 U.S.C. 103 (a) as being unpatentable over Hetherington et al. (U.S. Patent No. 5,978,864) in view of Shiell et al. (U.S. Patent No. 6,138,232). Applicants submit that the present claims are patentable over Hetherington in view of Shiell.

Hetherington discloses a system and method for thermal overload detection and protection for an integrated circuit processor. The system allows the processor to run at near maximum potential for the vast majority of its execution life. This is effectuated by the provision of circuitry to detect when the processor has exceeded its thermal thresholds and which then causes the processor to automatically reduce the clock rate to a fraction of the nominal clock while execution continues. When the thermal condition has stabilized, the clock may be raised in a stepwise fashion back to the nominal clock rate. See Hetherington at col. 3, ll. 53-65.

Moreover, the system discloses a thermal sensing circuit that incorporates a programmable threshold which, when reached, causes the circuit to generate a non-masked interrupt to the processor which may be identical to a power down "Energy Star" interrupt. The internal phase-locked loop ("PLL") clock dividers may be employed to

step down the master clock from nominal to, for example, 1/64.sup.th of the nominal rate. Program execution would then continue at this lowered or reduced clock rate until the thermal sensing circuit again senses that a temperature threshold has been crossed, whereupon it may again issue a non-masked interrupt to raise the clock back to nominal frequency. As before, normal program execution commences at the conclusion of the interrupt (col. 4, ll. 42-58).

Nevertheless, Hetherington does not disclose or suggest power management logic to enable the CPU to execute a first quantity of instructions per cycle whenever the temperature of the CPU exceeds a predetermined threshold and to execute a second quantity of instructions per cycle whenever the temperature of the CPU is below the predetermined threshold.

Shiell discloses a method of operating a microprocessor. The microprocessor accepts an interrupt from one of a plurality of interrupt sources. The microprocessor then operates at a rate dependent upon the interrupt source. The rate of power consumption by the microprocessor corresponds to the selected rate of instruction operation. A rate table stores a table of interrupt source to rate of instruction operation. The rate table is accessed upon receipt of an interrupt to obtain a rate of instruction operation corresponding to the interrupt source. The microprocessors is then operated at the recalled rate. The rate table may be a read only memory or a read/write memory loaded upon initiation of the microprocessor. The rate of instruction operation may be controlled by a rate of instruction dispatch. For a superscalar microprocessor capable of concurrently executing plural instructions simultaneously the rate of instruction operation may be set by setting a number of instructions dispatched per instruction cycle. This could include dispatching instructions to a number of execution units based upon the selected rate. Electric power consumption is conserved by powering only those execution units to which instructions are dispatched. See Shiell at col. 1, ll. 45 – col. 2, ll. 25.

Applicants submit that Shiell also fails to disclose or suggest power management logic to enable the CPU to execute a first quantity of instructions per cycle whenever the temperature of the CPU exceeds a predetermined threshold and to execute a second quantity of instructions per cycle whenever the temperature of the CPU is below the predetermined threshold.

Claim 1 recites:

> A system comprising a central processing unit (CPU) including power management logic to enable the CPU to execute a first quantity of instructions per cycle whenever the temperature of the CPU exceeds a predetermined threshold and to execute a second quantity of instructions per cycle whenever the temperature of the CPU is below the predetermined threshold.

As described above, neither Hetherington nor Shiell disclose or suggest such a limitation. As discussed above, Hetherington discloses circuitry to detect when a processor has exceeded its thermal thresholds, an in response causes the processor to automatically reduce the clock rate to a fraction of the nominal clock while execution continues. When the thermal condition has stabilized, the clock may be raised in a stepwise fashion back to the nominal clock rate. Meanwhile, Shiell discloses a microprocessor receiving an interrupt and operating at a rate dependent upon the interrupt source. Therefore, neither Hetherington nor Shiell disclose or suggest power management logic to enable a CPU to execute a first quantity of instructions per cycle whenever the temperature of the CPU exceeds a predetermined threshold and to execute a second quantity of instructions per cycle whenever the temperature of the CPU is below the predetermined threshold.

Since neither Hetherington nor Shiell disclose or suggest power management logic to enable the CPU to execute a first quantity of instructions per cycle whenever the temperature of the CPU exceeds a predetermined threshold and to execute a second quantity of instructions per cycle whenever the temperature of the CPU is below the

predetermined threshold, any combination of Hetherington and Shiell would also not disclose or suggest such a limitation.

Moreover, it is also respectfully submitted that Hetherington does not teach or suggest a combination with Shiell and that Shiell does not teach or suggest a combination with Hetherington. As discussed above, Hetherington includes a circuit that reduces processor power by reducing the processor clock rate to a fraction of the normal rate. Meanwhile, Shiell discloses a mechanism to service interrupts in a processor and operating at a rate dependent of the interrupt source.

Therefore, applicants submit that it would be impermissible hindsight based on applicant's own disclosure to incorporate the Shiell interrupt service mechanism into the Hetherington's thermal overload detection and prevention mechanism. Moreover, such a combination would still power management logic to enable the CPU to execute a first quantity of instructions per cycle whenever the temperature of the CPU exceeds a predetermined threshold and to execute a second quantity of instructions per cycle whenever the temperature of the CPU is below the predetermined threshold, any combination of Hetherington and Shiell would also not disclose or suggest such a limitation.

Accordingly claim 1 is patentable over Hetherington in view of Shiell. Claims 2-7 depend from claim 1 and include additional limitations. Therefore, claims 2-7 are also patentable over Hetherington.

Claim 8 recites:

> A method comprising:
> determining whether the temperature of a central processing unit (CPU) exceeds a predetermined threshold;
> executing a first quantity of instructions per cycle if the temperature of the CPU exceeds the predetermined threshold; and

executing a second quantity of instructions per cycle if the temperature of the CPU is below the predetermined threshold.

Therefore, for the reasons described above with respect to claim 1, claim 8 is also patentable over Hetherington. Since claims 9-15 depend from claim 8 and include additional limitations, claims 9-15 are also patentable over Hetherington.

Claim 16 recites

A central processing unit (CPU) comprising:
a thermal sensor; and
an instruction execution unit to generate a first quantity of instructions per cycle in a first execution mode whenever the thermal sensor measures temperature exceeding a predetermined threshold and to generate a second quantity of instructions per cycle in a second execution mode whenever the thermal sensor measures temperature below the predetermined threshold.

Thus, for the reasons described above with respect to claim 1, claim 16 is also patentable over Hetherington. Since claims 17-19 depend from claim 16 and include additional limitations, claims 17-19 are also patentable over Hetherington.

Claim 20 recites:

Power management logic comprising:
a thermal sensor; and
an instruction execution unit to generate a first quantity of instructions per cycle in a first execution mode whenever the thermal sensor measures a temperature exceeding a predetermined threshold and to generate a second quantity of instructions per cycle in a second execution mode whenever the thermal sensor measures temperature below the predetermined threshold; and
interrupt generating hardware to generate a first interrupt whenever the thermal sensor measures a temperature that exceeds the predetermined threshold and generates a second interrupt whenever the thermal sensor measures a temperature below the predetermined threshold.

Accordingly, for the reasons described above with respect to claim 1, claim 20 is also patentable over Hetherington. Since claims 21-24 depend from claim 20 and include additional limitations, claims 21-24 are also patentable over Hetherington.

Claims 4-7 stands rejected 35 U.S.C. 103 (a) as being unpatentable over Hetherington et al. (U.S. Patent No. 5,978,864) in view of Shiell et al. (U.S. Patent No. 6,138,232) and further in view of McFarland et al. (U.S. Patent No. 5,125,093). Applicants submit that the present claims are patentable over Hetherington and Shiell even in view of McFarland.

McFarland discloses a technique of servicing interrupts among a plurality of microprocessors. See McFarland at Abstract. Nevertheless, McFarland does not disclose or suggest power management logic to enable the CPU to execute a first quantity of instructions per cycle whenever the temperature of the CPU exceeds a predetermined threshold and to execute a second quantity of instructions per cycle whenever the temperature of the CPU is below the predetermined threshold, any combination of Hetherington and Shiell would also not disclose or suggest such a limitation.

As discussed above, neither Hetherington nor Shiell disclose or suggest such a limitation. Therefore, any combination of Hetherington, Shiell and McFarland would also not disclose or suggest power management logic to enable the CPU to execute a first quantity of instructions per cycle whenever the temperature of the CPU exceeds a predetermined threshold and to execute a second quantity of instructions per cycle whenever the temperature of the CPU is below the predetermined threshold, any combination of Hetherington, Shiell and McFarland would also not disclose or suggest such a limitation. Accordingly, the present claims are patentable over Hetherington and Shiell in view of McFarland.

Applicants respectfully submit that the rejections have been overcome, and that the claims are in condition for allowance. Accordingly, applicants respectfully request the rejections be withdrawn and the claims be allowed.

The Examiner is requested to call the undersigned at (303) 740-1980 if there remains any issue with allowance of the case.

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,
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